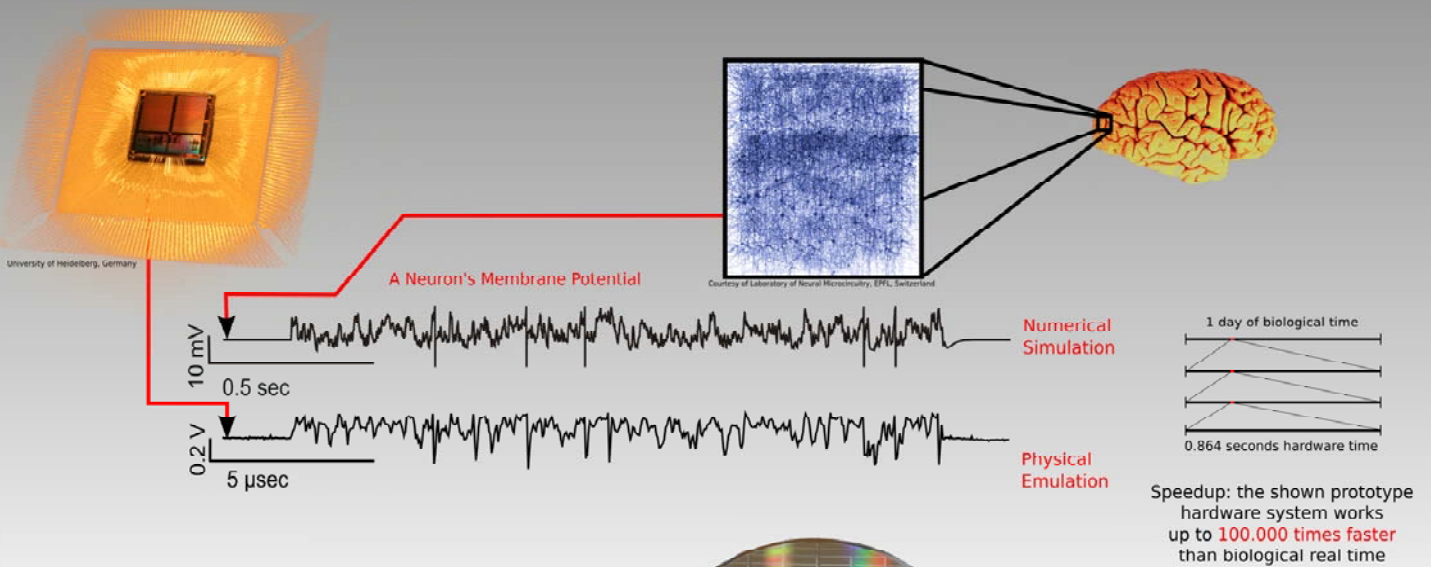


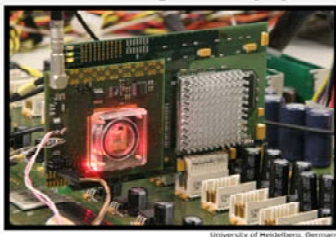
Biological Experiments at the Cell Level	Biological Experiments at the Network Level
Modeling and Databases at the Cell Level	Modeling and Databases at the Network Level
Neuromorphic Hardware at the Cell Level	Neuromorphic Hardware at the Network Level

 <p>Biological Experiments</p>	 <p>Theoretical Studies and Computer-based Models</p>	 <p>High Precision Neuromorphic Hardware Systems</p>	 <p>Large Scale Neuromorphic Hardware Systems</p>
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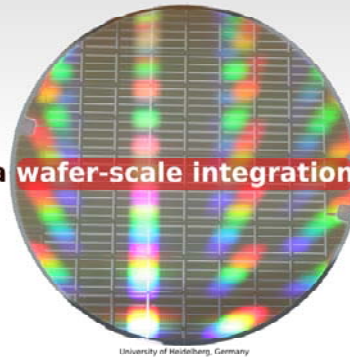
Building and Using Highly Accelerated Hardware Models to Study Cortical Circuits



From a single-chip prototype...

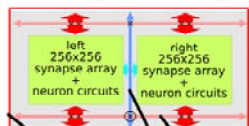


... towards a wafer-scale integration system



Neural Network Chip

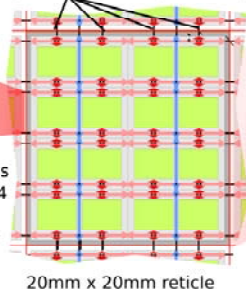
- Conductance-based integrate-and-fire neuron model
- Low-power analog VLSI implementation
- 131,072 synapses, to up to 512 neurons
- ~10,000 x faster than biological real-time
- Built-in synaptic learning



256 horizontal bus lanes
 64 vertical bus lanes w/64 spike sources per lane
 Repeaters w/timing recovery for chip-to-chip communication

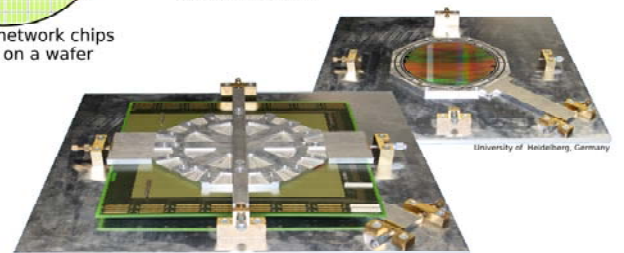
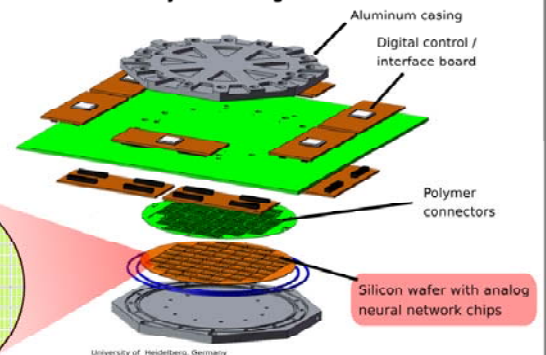
Wafer-Scale Integration

- 8 network chips per 20mm x 20mm reticle
- High-bandwidth connections between chips via parallel LVDS continuous-time bus system
- Signalling across reticle boundaries realized by separate **post-processing** metal layer



Approx. 450 network chips integrated on a wafer

System Design



Contact "Large Scale Neuromorphic Hardware":

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