Building and Using Hardware Models to Study Cortical Circuits

From a single-chip prototype... ...towards a wafer-scale integration system

Neural Network Chip
- Conductance-based integrate-and-fire neuron model
- Low-power analogous VLSI implementation
- 131,072 synapses, up to 512 neurons
- 10,000 faster than biological real-time
- Built-in synaptic learning

Wafer-Scale Integration
- 8 network chips per 20mm x 20mm reticle
- High-bandwidth connections between chips via parallel VLSI continuous-time bus system
- Signalling across reticle boundaries realized by separate post-processing metal layer

System Design
- Aluminum casing
- Polymer connectors
- Digital control / interface board
- Silicon wafer with analog neural network chips

Relation to Nanotechnology?
Neural Architectures exhibit fault tolerance and self organization
These features are key requirements for systems built with low yield nanocomponents