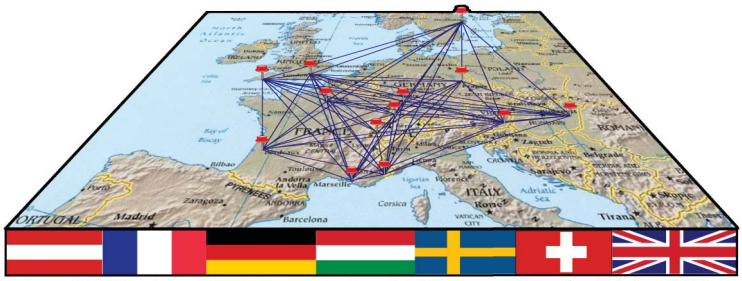
FACETS

http://www.facets-project.org

Fast Analog Computing with Emergent Transient States

What is FACETS?
- European joint research project
- 15 partners in 7 countries
- Funded by European Commission within Sixth Framework Programme

Goals
- To explore information processing in the brain
- To build neuromorphic hardware models of substantial parts of the cortex
- **To perceive novel computing paradigms going beyond conventional IT systems based on the Turing model**

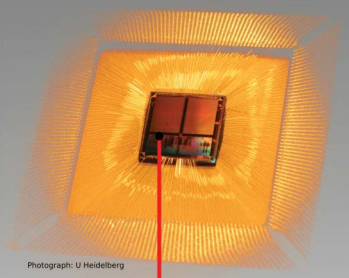


Partners: ENSEIR Bordeaux, CNRS (Gif-sur-Yvette, Marseille), U Debrecen, TU Dresden, U Freiburg, TU Graz, U Heidelberg, EPFL Lausanne, U London, U Plymouth, INRIA, KTH Stockholm

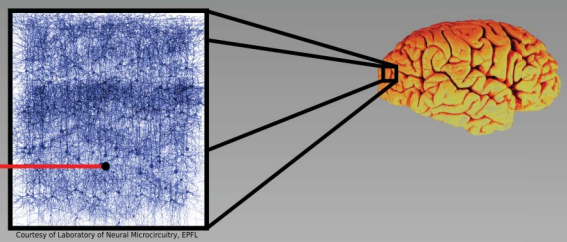
Contact in Japan: Abigail Morrison, Markus Diesmann {abigail,diesmann}@brain.riken.jp

Biological Experiments | Theoretical Studies and Computer-based Models | **Neuromorphic Hardware** | Emerging Computational Paradigms

Building and Using Hardware Models to Study Cortical Circuits

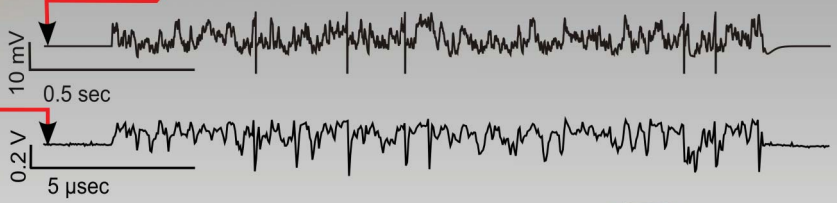


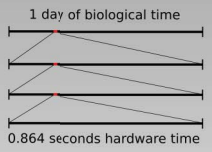
Photograph: U Heidelberg



Courtesy of Laboratory of Neural Microcircuitry, EPFL

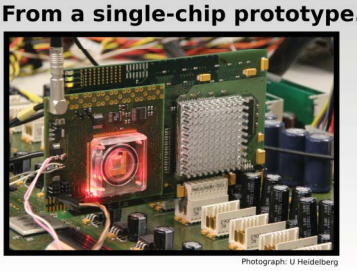
A Neuron's Membrane Potential





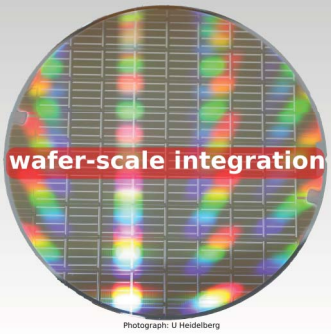
Speedup: the shown prototype hardware system works up to 100.000 times faster than biological real time

From a single-chip prototype...



Photograph: U Heidelberg

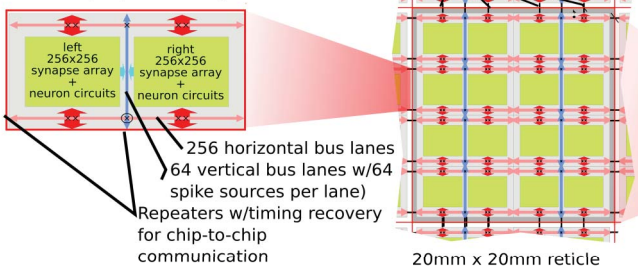
... towards a wafer-scale integration system



Photograph: U Heidelberg

Neural Network Chip

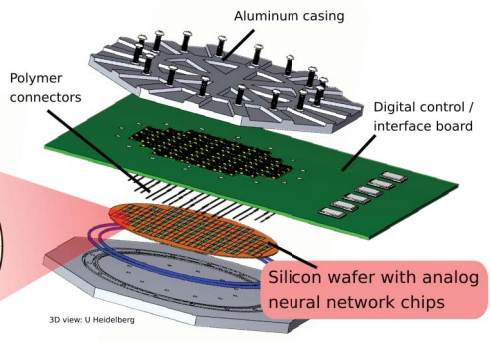
- Conductance-based integrate-and-fire neuron model
- Low-power analog VLSI implementation
- 131,072 synapses, to up to 512 neurons
- ~10,000 faster than biological real-time
- Built-in synaptic learning



Wafer-Scale Integration

- 8 network chips per 20mm x 20mm reticle
- High-bandwidth connections between chips via parallel LVDS continuous-time bus system
- Signalling across reticle boundaries realized by separate **post-processing** metal layer

System Design



Relation to Nanotechnology?

Neural Architectures exhibit fault tolerance and self organization

These features are key requirements for systems built with low yield nanocomponents