FACETS

FP6-2004-IST-FETPI 15879

Fast Analog Computing with Emergent Transient States

Hardware specifications for the next generation of neural ASIC circuits

Report Version: 1.0

Report Preparation: Jean Tomas, Sylvie Renaud, Alain Destexhe

Classification: Pub

Contract Start Date: 01/09/2005 Duration: 4 Years

Project Coordinator: Karlheinz Meier (Heidelberg)

Partners: U Bordeaux, CNRS (Gif-sur-Yvette, Marseille), U Debrecen, TU Dresden, U Freiburg, TU Graz, U Heidelberg, EPFL Lausanne, Funetics S.a.r.l., U London, U Plymouth, INRIA, KTH Stockholm

Project funded by the European Community under the "Information Society Technologies" Programme

DELIVERABLES TABLE

Project Number: ***FP6-2004-IST-FETPI 15879***

1) Project Acronym: FACETS

Title: ***Fast Analog Computing with Emergent Transient States***

Del. No.	Revision	Title	Type[1]	Classification[2]	Due Date	Issue Date
18	**1.0**	**Hardware specifications for the next generation of neural ASIC circuits**	**R**	**Pub**	**31/08/06**	**15/09/06**

[1] *R: Report; D: Demonstrator; S: Software; W: Workshop; O: Other – Specify in footnote*

[2] *Int.: Internal circulation within project (and Commission Project Officer + reviewers if requested)*
Rest.: Restricted circulation list (specify in footnote) and Commission SO + reviewers only
IST: Circulation within IST Programme participants
FP5: Circulation within Framework Programme participants
Pub.: Public document

DELIVERABLE SUMMARY SHEET

Project Number: FP6-2004-IST-FETPI 15879

Project Acronym: FACETS

Title: Fast Analog Computing with Emergent Transient States

Deliverable N°:	18
Due date:	31/08/06
Delivery Date:	15/09/06

Short description:

The mixed analog-digital neural simulator developed in WP6 is based on ASICs that are controlled by a software /hardware custom environment. These ASICs are the analog core of the simulator, and compute the activity of artificial neurons, modeled using .a conductance-based representation (Hodgkin-Huxley formalism). The ASICs are full custom analog circuits designed in a sub-micron SiGe technology. This report presents the first generation of circuits designed and fabricated during the first year of the project and identifies the key points that will be addressed in the next generation to improve their functionality.

Partners owning: ENSEIRB (3)

Partners contributed: : ENSEIRB (3) CNRS (6a)

Made available to: all

I. OVERVIEW

This report details the execution of the Task2 described in WP6. For this task, neuron models that will be implemented in hardware have to be defined, as a collaborative effort between biologist that evaluate their biological relevance, computational neuroscientist that process preliminary simulations of the models, and physicist that will design the VLSI circuits computing the models in hardware. We will describe in this report first the Hogkin-Huxley formalism and the chosen neural element model, then how this formalism has been integrated into an ASIC (Application Specific Integrated Circuit) called "Galway". At last, we propose several new specifications for the future ASICs generations, to better fit different neuron activities.

II. HOGKIN-HUXLEY FORMALISM

The electrical activity of a neuron is the consequence of the diffusion of ionic species through its membrane. This activity is characterized by a membrane potential which is the voltage differential between the outside and the inside of the cell. Ions flow through the cell membrane through an ion-specific channel, generating ionic currents. An equilibrium potential is associated with each ion type, according to the difference between the intracellular and extracellular concentrations. For each ion type, the fraction of the opened channels determines the global conductance of the membrane of that ion. This fraction results from the interaction between time and voltage dependent activation and inactivation processes.

The Hodgkin-Huxley formalism proposes a set of equations and an electrical equivalent circuit (Fig. 1) that describe these phenomena. The current flowing across a membrane is integrated on the membrane capacitance, following the electrical equation (1),

$$C_{MEM}\frac{dV_{MEM}}{dt} = -\sum_{i} I_{ION} + I_S \quad (1)$$

where V_{MEM} is the membrane potential, C_{MEM} the membrane capacitance and I_S stimulation and synaptic current

I_{ION} is the current passing through the specific ionic channels, I_{ION} is given by (2), in which g_{max} is the maximal conductance value, m (opening/activation) and h (closing/inactivation)

are the dynamic functions describing the permeability of membrane channels to this ion, V_{EQUI} the equilibrium potential and p,q integers.

$$I_{ION} = g_{max}\, m^p\, h^q\, (V_{MEM} - V_{EQUI}) \quad (2)$$

As shown in (3), m converges to its associated steady-state value m_∞, which is a sigmoïdal function of V_{MEM}. The time constant for the convergence is τ_m. V_{OFFSET} is the activation sigmoïde offset and V_{SLOPE} the activation sigmoïde slope. The variable h follows the same dynamics, with an inversely sigmoïdal steady-state value h_∞ .

$$\tau_m(V_{MEM})\frac{dm}{dt} = m_{inf}(V_{MEM}) - m \qquad m_{inf}(V_{MEM}) = \frac{1}{1+\exp\left(-\dfrac{V_{MEM} - V_{OFFSET\_M}}{V_{SLOPE\_M}}\right)} \quad (3)$$

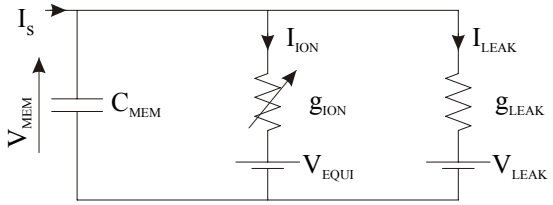

Fig. 1: Neuron electrical equivalent circuit

III. NEURAL ELEMENT

The chosen structure of the neural element presents digital inputs and one digital output while all the variables represented by membrane voltage and ionic or synaptic currents are analog and computed in continuous time. The structure of a neuron unit is shown in Fig. 2. The pre-synaptic signal named ‘ Synaptic Trig’ is triggering the synaptic currents. The action potentials output by this analog neuron are then detected and used to generate an output digital signal, called S (“neuron activity”). A configuration data bus is also present to be able to tune the parameters values of both synaptic and ionic currents.

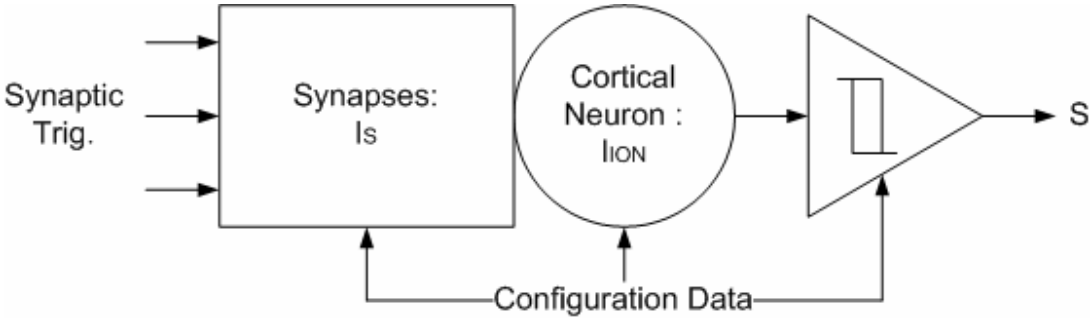

Fig. 2 : Neural element structure

A computer is used to collect and dispatch the digital signals according to the connectivity rules, which are completely software-controlled. As analog neurons are integrated separately, and perform parallel computation, the size limitation (number of neurons) of the system only depend of the computer constraints (data transfer latency and software).

In the equation (1) of Hogkin-Huxley formalism, two main different types of current are presents : ionic currents and synaptic currents

Each ionic current generator (or conductance) is built according to synoptic Fig.3, where each parameter input is connected to its electrical image in an internal way for voltages and currents, in an external way for any time constant.

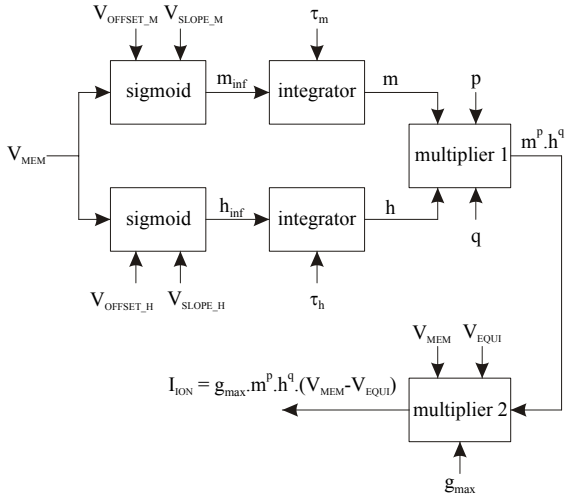

Fig. 3 : Modular structure of the integrated ionic current generator

One limitation we have introduced in our integrated model is to fix the value of time constants τ_h and τ_m, that are no more depending of the membrane potential.

We chose to model synaptic interactions using "exponential" synapses, where the synaptic conductance increases of a given "quantal conductance" when a presynaptic spike occurs, then relaxes exponentially to zero (Destexhe and al., 1994). The associated post-synaptic current I_{SYN} is given in (4) and (5), where g_{MAX} is the maximal conductance, E_{SYN} the reverse synaptic potential, V_{MEM} the post-synaptic membrane potential, r the fraction of receptors in open state, α and β voltage-independent forward and backward rate constants, [T] the transmitter concentration

$$I_{SYN} = g_{MAX}\ r\ (V_{MEM} - E_{SYN}) \quad (4) \qquad \frac{dr}{dt} = \alpha[T](1-r) - \beta r \quad (5)$$

Fig. 4 illustrates the time-variation of the synaptic conductance g when a transmitter concentration pulse [T] occurs, assuming that the transmitter is released when a presynaptic action potential appears. As the quantum Δg is proportional to the Δt pulse width, this later parameter will be exploited to modulate Δg.

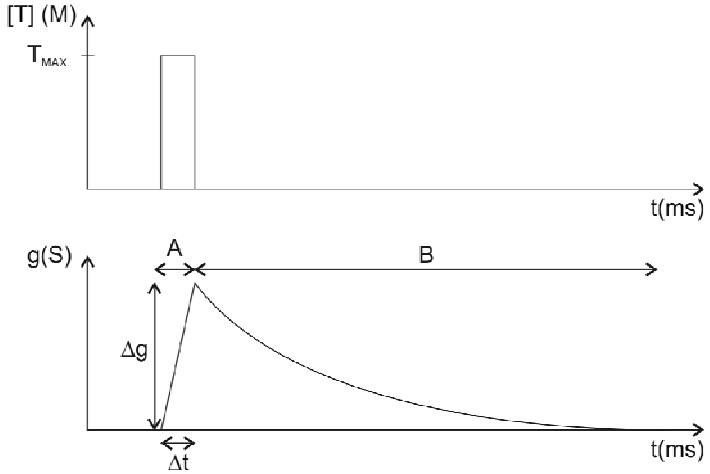

Fig. 4: Exponential decay synapse principle

Furthermore, synaptic summation, which occurs when multiple pre-synaptic spikes are simultaneously presented, will be handled naturally by the integration of successive transmitter pulses. The time constants and quantum sizes can be adjusted to fit experimental recordings of excitatory (glutamatergic, AMPA) and inhibitory (GABAergic) synaptic currents. The encoding of the conductance quantum, which represents the synaptic strength, is done by modulating the pulse duration. The modulation is digitally controlled. As long as the signal is active on the input, the synaptic conductance increases. When the input signal stops (end of the 'pulse'), the conductance decreases exponentially. This synapse model is

particularly well adapted for an electronics implementation: it aggregates multiple synaptic inputs in a unique mechanism, and therefore limits the hardware connections.

IV. ASIC INTEGRATION

We have decided to use austria*micro*systems (AMS) BiCMOS 0.35µm technology to integrate all the ASICs designed during FACETS contract. This choice has been motivated by the permanence of this technology and by a reasonable cost (around 1000€ per mm² of design). The first ASIC is called "Galway" and we will detail its content in this paragraph.

To improve the dynamics of the electrical simulator, we have chosen to multiply the biological value of ionic currents and voltages by different ratios. The values of these ratios are indicated in Table 1. Time scale is not modified, so time constants keep the same value for both biological and electrical models.

	Biological	Electrical	Ratio
Currents	1nA	50nA	x50
Voltages	100mV	500V	x5
Conductances	1mS	10mS	x10
Capacitances	1nF	10nF	x10

Table 1

Let us notice that the ratios of conductance and capacitance are deducted from the two previous ones.

Keeping in mind that the area of the integrated cells is 0.00022cm2 (which corresponds to a value for the membrane capacitance CMem=1µF/cm2), the membrane capacitor has a value C_{MEM}=0.22nF in the biological domain, so we connect a 2.2nF capacitor to the V_{MEM} output of our circuit.

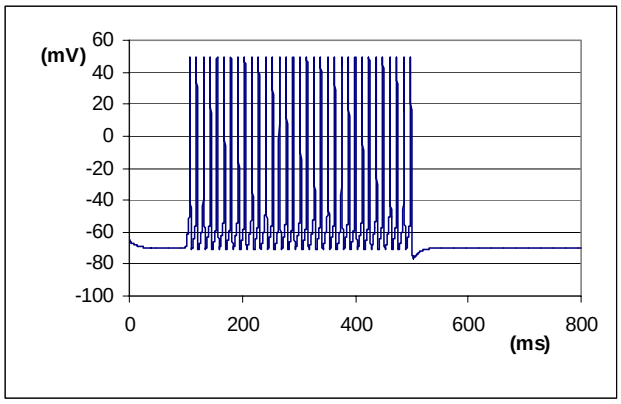

Fig.5: Numerical simulation of inhibitory neuron (FS)

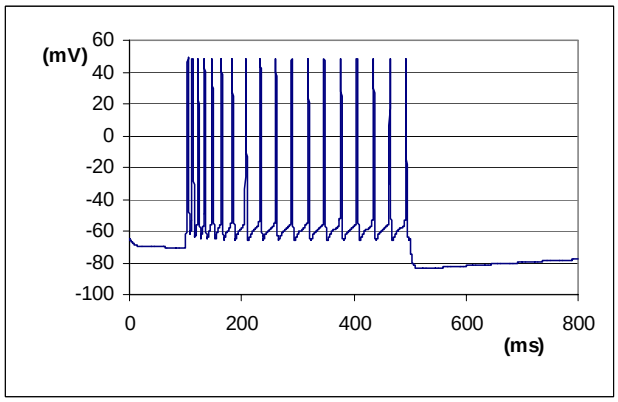

Fig. 6: Numerical simulation of excitatory neuron (RS)

We used 2 generic models for excitatory and inhibitory neurons based, according to the classification of Connors and Gutnick (1990). All the neurons contain a leak conductance and voltage-dependent Na and K conductances, necessary to generate action potentials. This model reproduces the "fast spiking" phenotype (Fig. 5), which represents the major class of inhibitory neurons in different cortical areas as well as in many other parts of the central nervous system. Another important class of neurons in the cerebral cortex is the one of excitatory neurons ("regular-spiking" phenotype - Fig. 6). Their model includes an additional slow voltage-dependent K current (I_M) responsible for spike-frequency adaptation. Simulations are run using the NEURON software (Hines et al., 1997)

As precise models and types of neurons were not available during the design of "Galway", the circuit is organized to provide to user a large variety of configurations for the simulated neural network. As the neural activity is generated by a sum of ionic and synaptic currents on a membrane capacitance, we decided to integrate a set of generic blocks, each able to compute a conductance-based model of ionic or synaptic current. During the configuration phase, the user will also set the topology of the network, i.e. define the blocks connectivity. A set of connected blocks will form a neural element, with their respective currents summed on an external capacitor. The structure of "Galway" chip is described in Fig. 7.

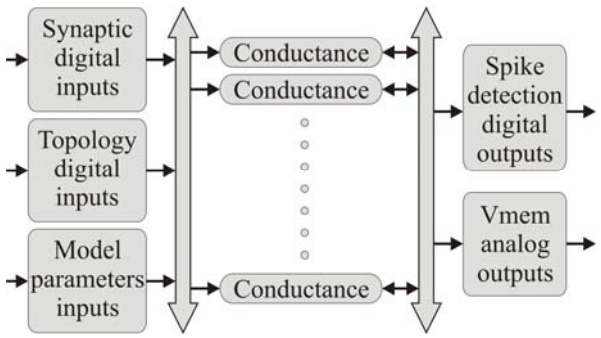

Fig.7: structure of "Galway" chip

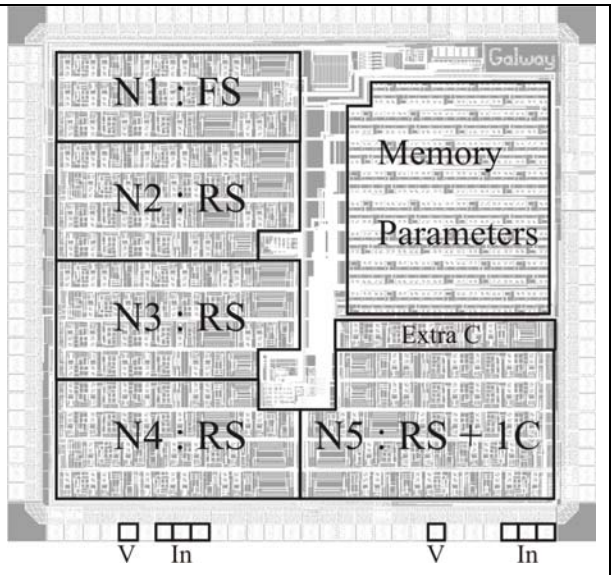

Fig.8 : layout of "Galway" chip

The *Galway* chip we present here comprises (Fig 7):

- a set of conductance modules, each able to generate an ionic or synaptic current following the conductance-based model

- spike-detection modules, to code on 1-bit the neuron membrane voltage

- Vmem analog output for each neuron

- a set of synaptic input modules, that activate synaptic conductance modules with a digitally-controlled weight

- an analog memory cells array, to store the model parameters

- a matrix of switches, to control the neurons topology (i.e. the arrangement of the conductance and synaptic modules that form the artificial neuron)

- digital functions to control data transfer from and to external devices.

All the parameters of the model card of any type of inhibitory or excitatory neurons are stored into an internal analog memory cell array except the time constants that required external capacitors. The analog memory cells are refreshed every 2ms via a serial input managing the model parameters input. The analog functions like sigmoid, integrator and multiplier had been designed in such a way that their inputs are compatible with the full range variation of parameters.

"Galway" integrates 5 neural elements, each of them has 3 synaptic current – one for inhibitory input, one for excitatory input and one for background noise activity.

Due to the biological ratio of inhibitory and excitatory cells, we have integrated, as shown in the layout of "Galway" depicted in Fig.8 :

- 1 Fast Spiking cell (N1) constructed with 3 conductances I_{leak}, I_{Na}, I_K
- 3 Regular Spiking cells (N2,N3,N4) with 4 conductances I_{leak}, I_{Na}, I_K, I_M
- 1 Regular Spiking cell (N5) with a fifth conductance identical to I_M.
- 1 extra conductance identical to I_M, that can be connected either to N4 either to N5
- the memory cell array storing the parameters of the neuron model card

The area of the chip is 10.5 mm2, and it is composed by 47000 devices.

At this moment, we perform functional tests on "Galway" and we obtain good behavior. Fig. 9 and Fig. 10 respectively illustrates spiking activity with typical value of parameters and exponential decay synapse waveform.

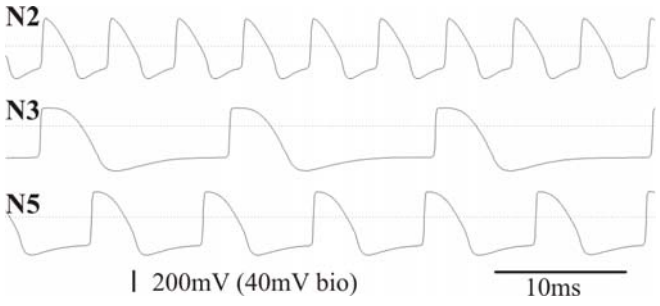

Fig. 9: spiking activity of neurons N2, N3 & N5 of "Galway"

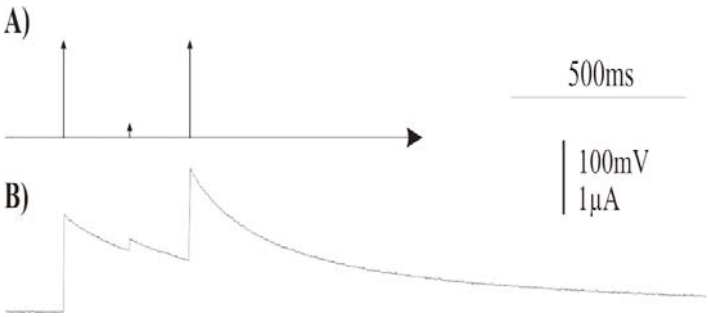

Fig. 10: A) digital synaptic weight
B) exponential decay wave form of a synapse

V. SPECIFICATION OF NEXT GENERATION ASIC

The ASICs of the next generation will have to fit different electrical activities that are described below. These models had been provided at the Facets Plasticity Workshop by Alain Destexhe.

In the category of inhibitory cells (Fig. 11), we may observe the classical Fast Spiking neuron composed by 3 conductances I_{leak}, I_{Na}, I_K ; adding an anomalous rectifier channel called I_h we obtain the Slow Firing activity ; adding two currents a low threshold calcium current called I_{CaT} and a transient potassium current called I_{si} we obtain stuttering activity.

In the category of excitatory cells (Fig. 12), we may observe the classical Regular spiking neuron composed by I_{leak}, I_{Na}, I_K, I_M ; adding one more current i.e. a low or high threshold calcium current I_{CaT} or I_{CaL} we obtain different activities called Intrinsically Bursting or Rebound Bursting or Repetitive Bursting.

Many of these neurons need 5 conductances. Moreover, as our integrated model only manages fixed time constant for τ_h and τ_m , we have tried to find such value. In the case of I_{si} and I_h the best fit is obtained using a step function and not a fixed value; for instance I_{si}, τ_h = 20 ms for $V_{mem} \leq$ -49 mV and τ_h = 80 ms for V_{mem} > 49 mV.

So, in conclusion, the next generation of ASIC should integrate :

- more neurons with 5 conductances
- step functions for specific time constant.

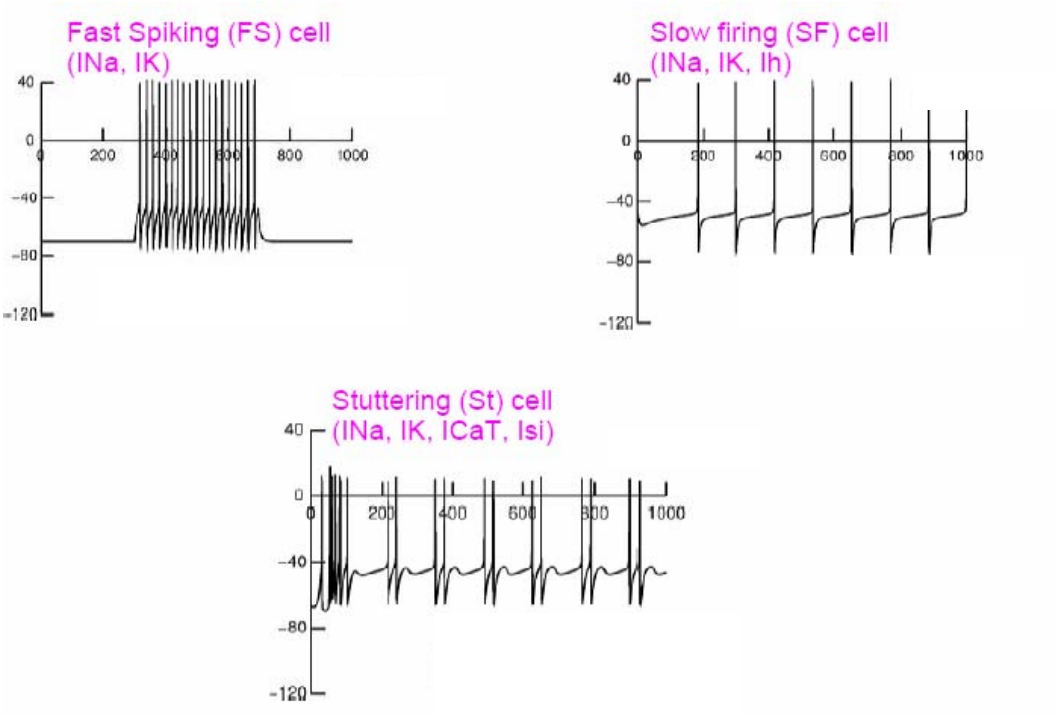

Fig. 11 : different activities for Fast Spiking (inhibitory) cells

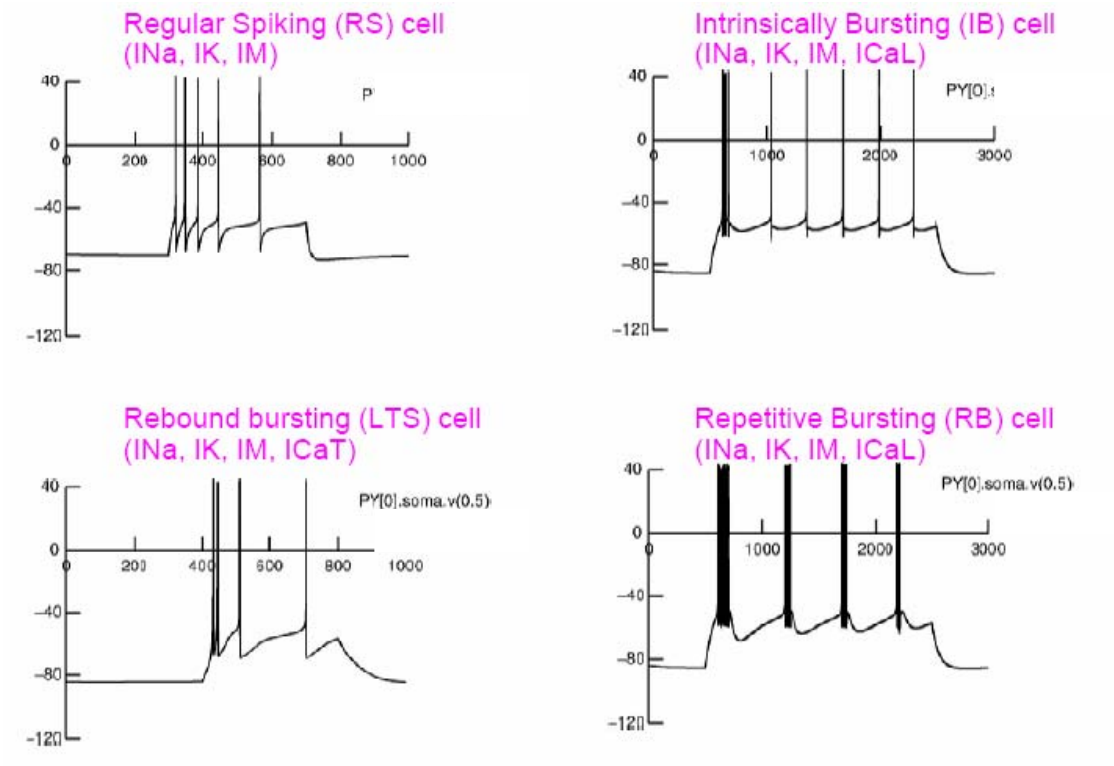

Fig. 12 : different activities for Regular Spiking (excitatory) cells

VI. REFERENCES

Destexhe, A., Mainen, Z.F. and Sejnowski, T.J., An efficient method for computing synaptic conductances based on a kinetic model of receptor binding. *Neural Computation* 6 : 14-18, 1994.

Connors, B.W. and Gutnick, M.J. Intrinsic Firing patterns of diverse neocortical neurons. *Trends Neurosci.* 13: 99-104, 1990.

Hines, M.L., Carnevale, N.T., The Neuron simulation environment. *Neural Computation*, 9 :1179-1209, 1997.