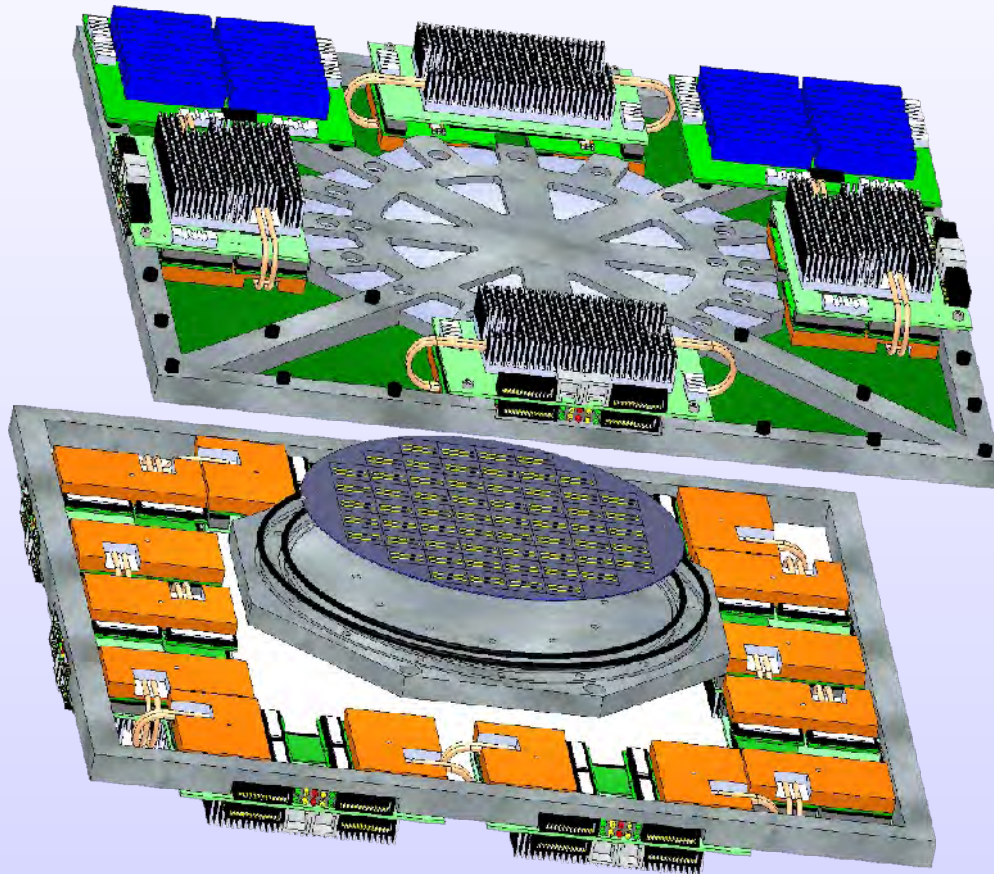


# Live Experiments: Implementing Network Models with the FACETS Hardware

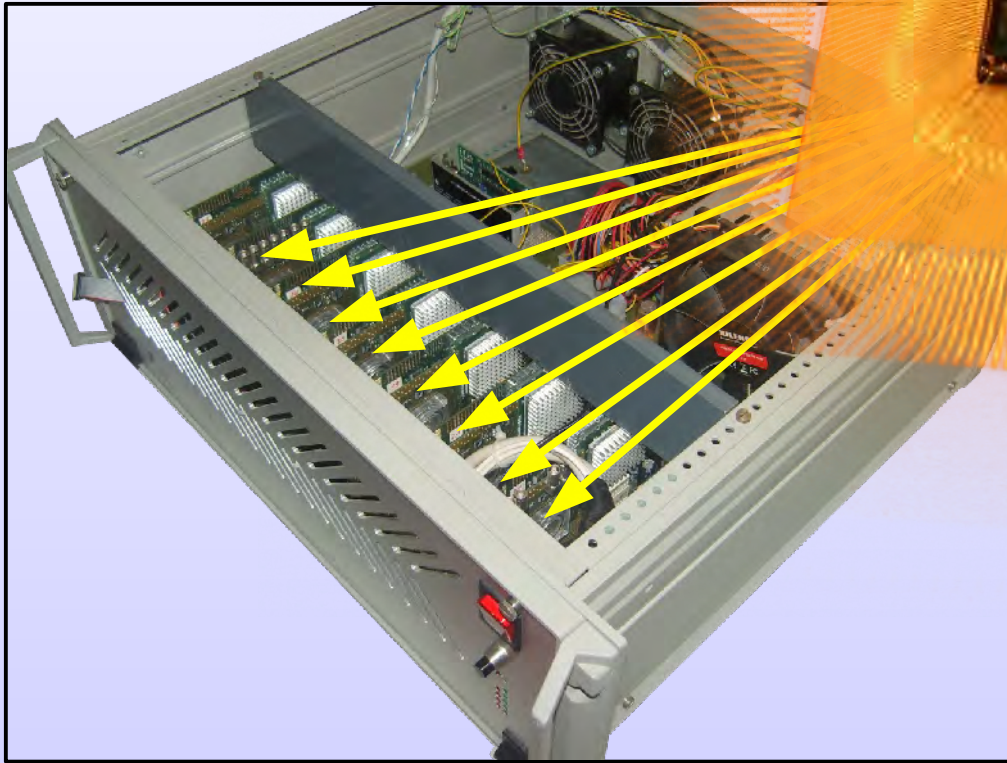
Daniel Brüderle  
Heidelberg

# The FACETS Wafer-Scale Hardware



**Up to 200.000 AdEx neurons**  
**50.000.000 plastic synapses**  
 **$10^4$  times faster than biological real time**

# The FACETS Stage I Chip

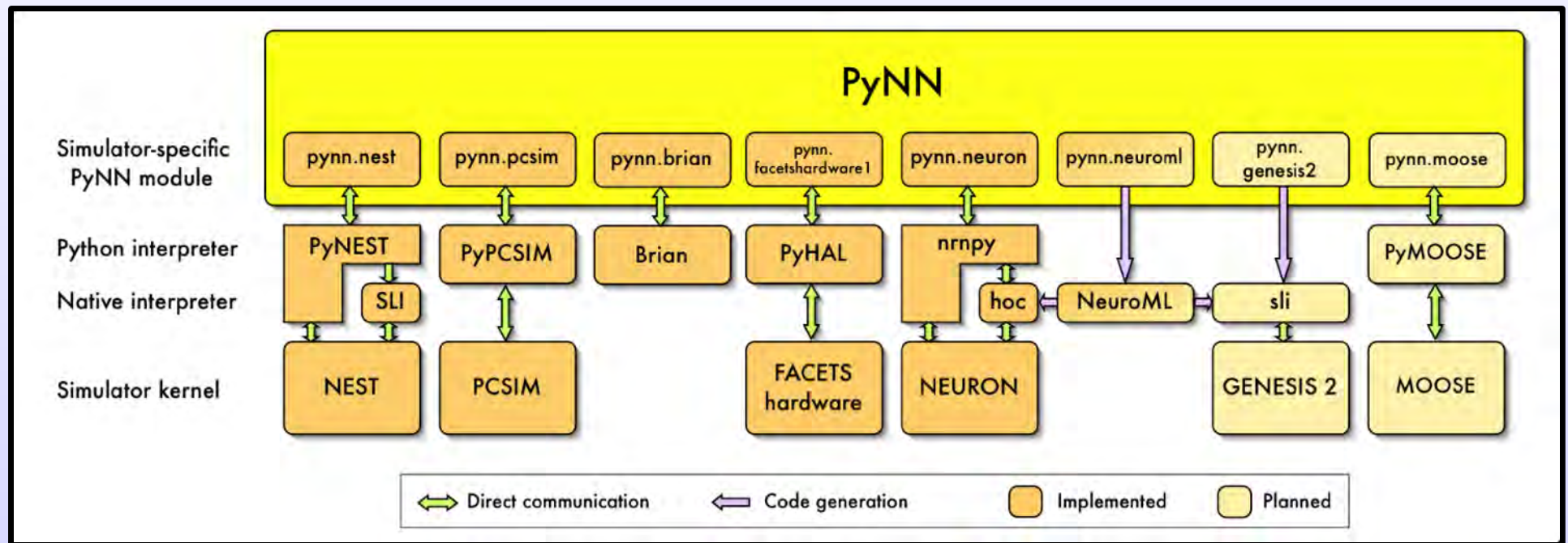


**384 leaky I&F neurons**  
**100.000 synapses**

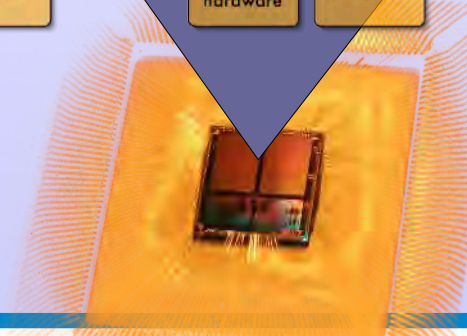
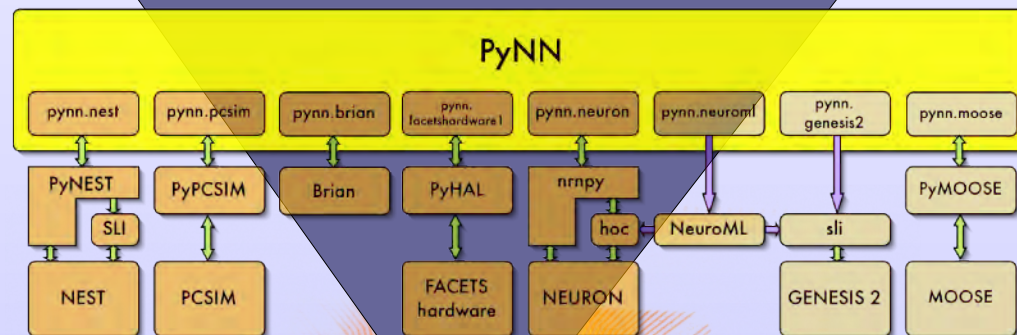
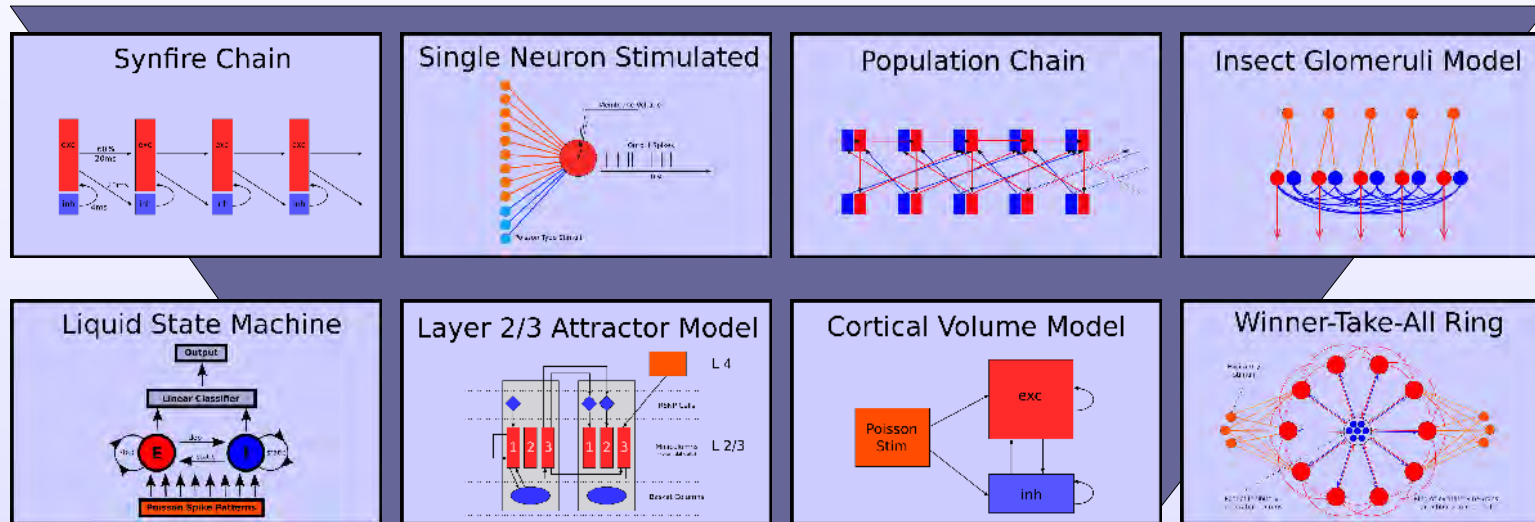
- programmable weights
- depression and facilitation
- STDP

**$10^4$  times faster than  
biological real time**

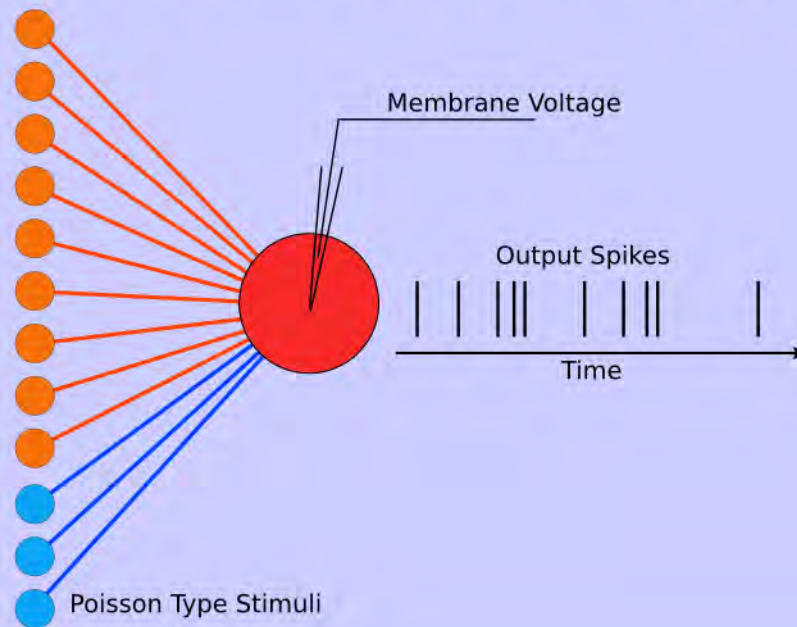
# Unified Interface Language for Multiple Software Simulators and the FACETS Hardware



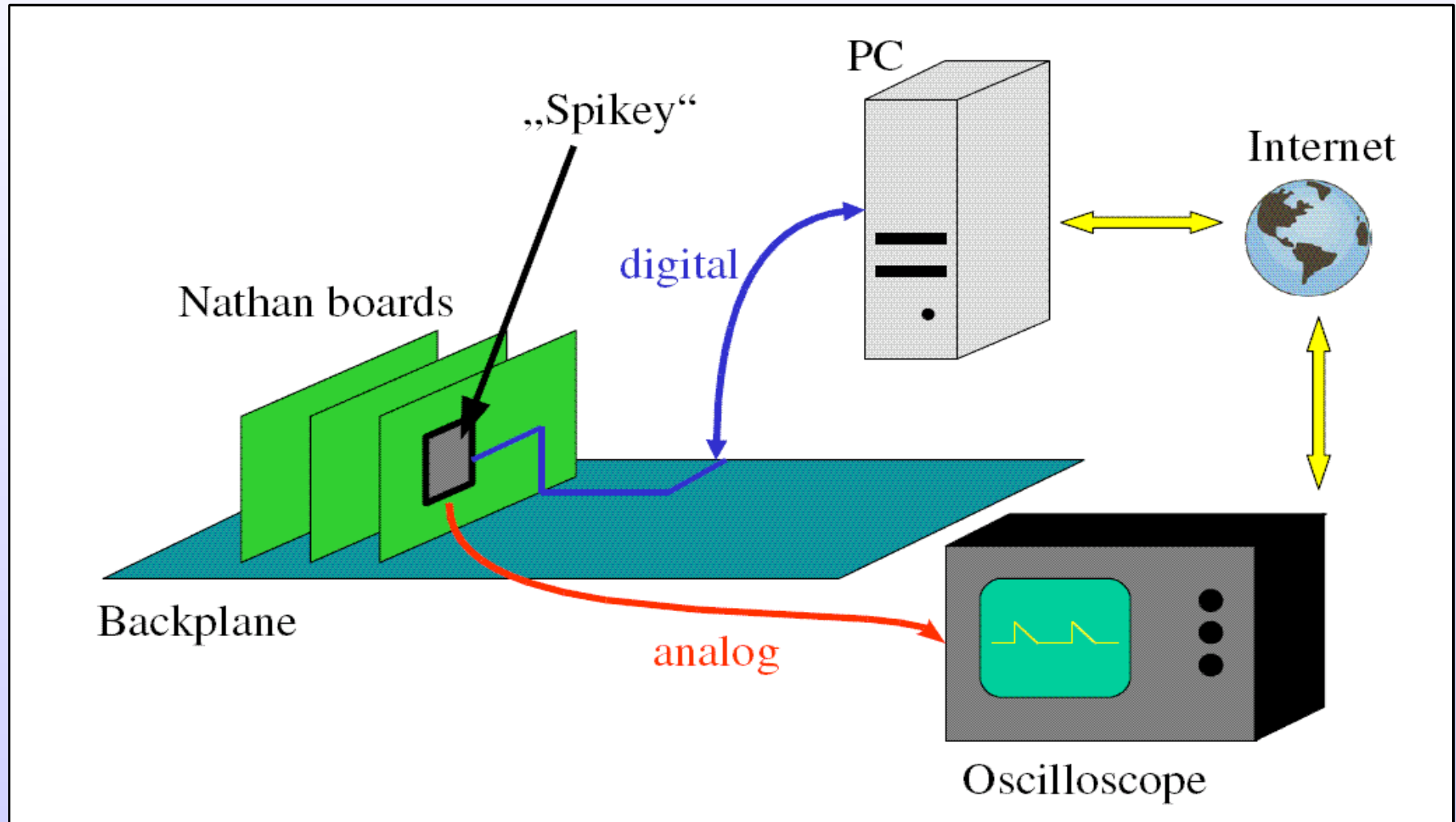
# Mapping Arbitrary Network Models to the FACETS Hardware



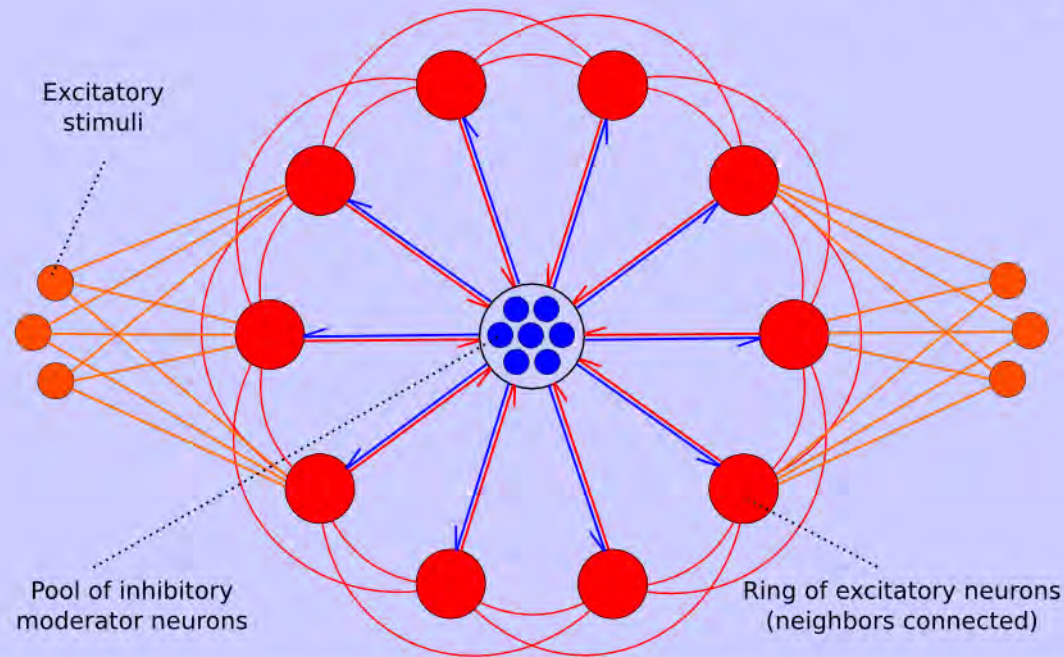
# Single Neuron Stimulated



# The FACETS Stage I System



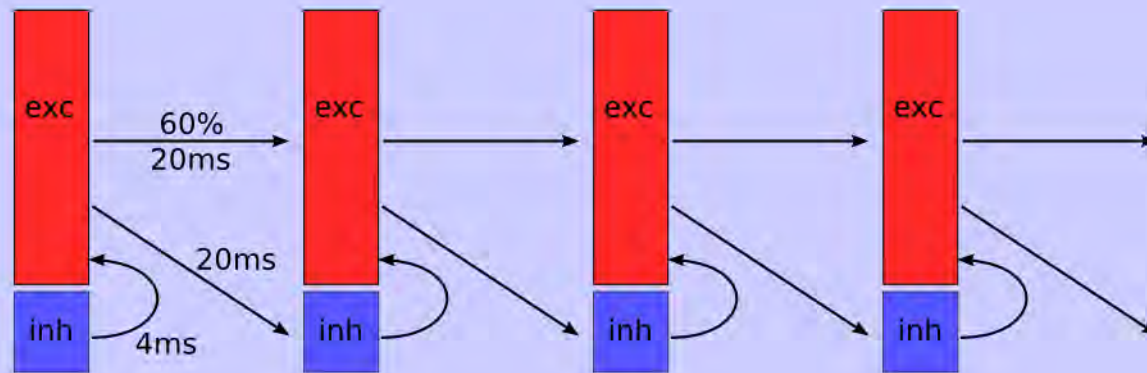
# Winner-Take-All Ring



*Modeling Orientation Selectivity Using a Neuromorphic Multi-Chip System.* Elisabetta Chicca, Patrick Lichtsteiner, Tobias Delbruck, Giacomo Indiveri and Rodney J. Douglas. ISCAS 2006. Hardware Implementation: D. Bruederle, E. Mueller

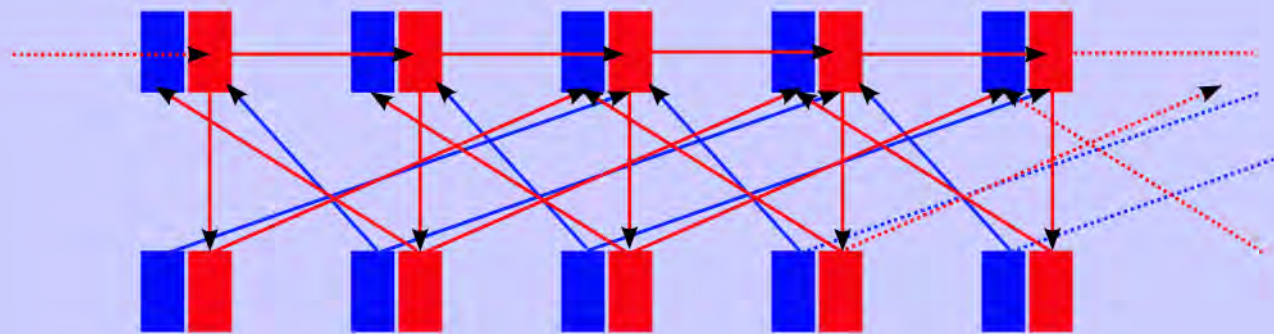


# Synfire Chain

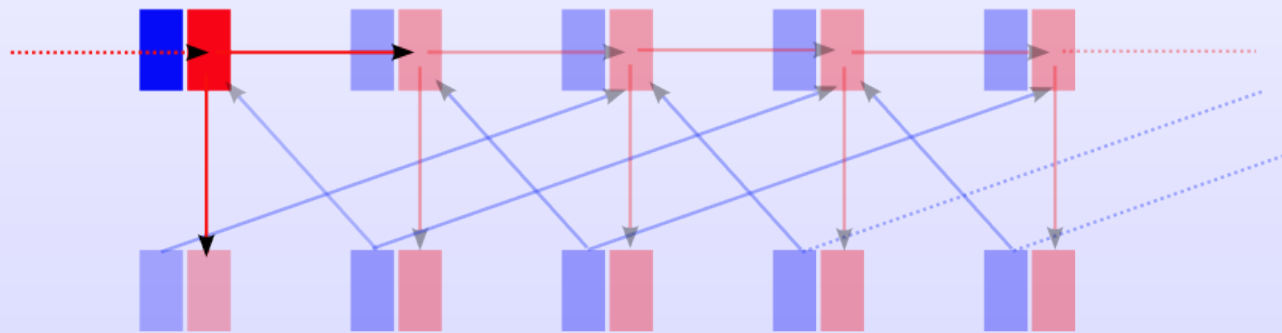


*Functional consequences of correlated excitatory and inhibitory conductances.* Kremkow, J., Perrinet, L., Aertsen, A. and Masson, G.S., Journal of Computational Neuroscience 2010  
Hardware Implementation: J. Kremkow, M. Petrovici

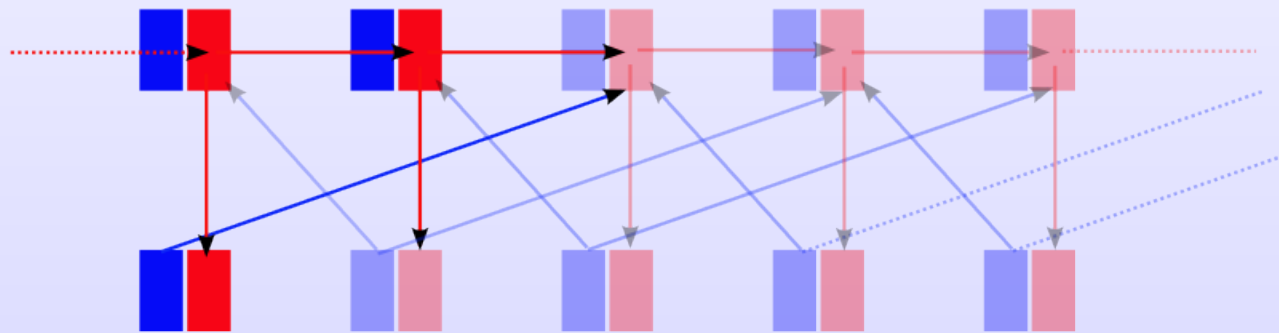
# Population Chain



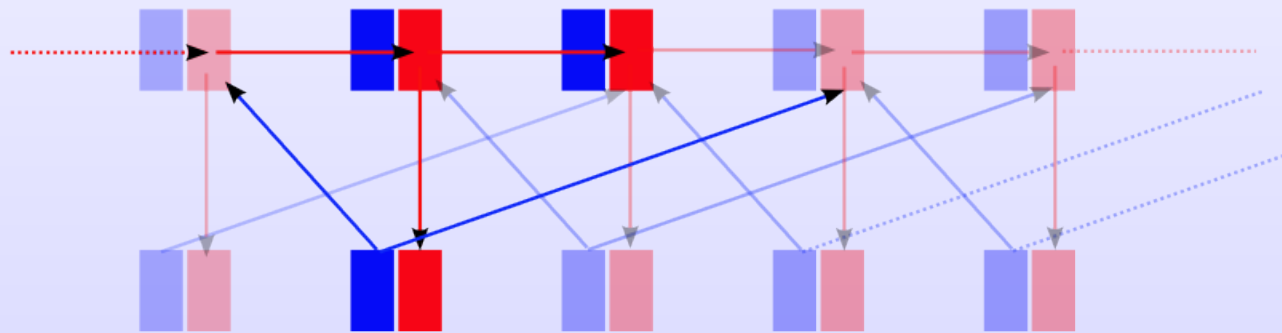
Concept: T. Clayton, D. Bruederle  
Hardware Implementation: T. Clayton, D. Bruederle



Concept: T. Clayton, D. Bruederle  
Hardware Implementation: T. Clayton, D. Bruederle

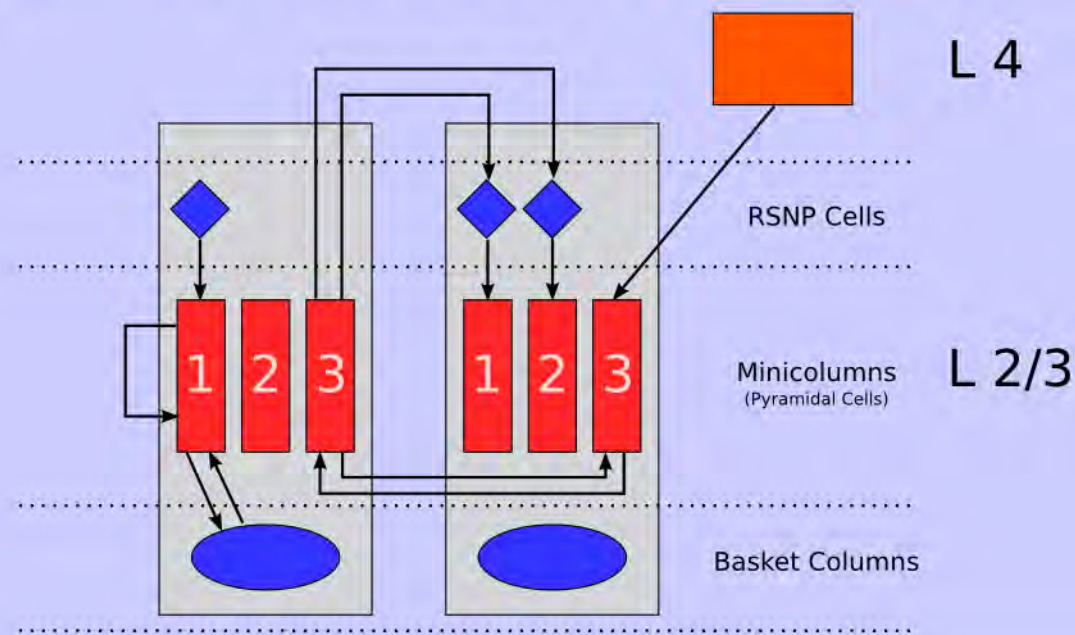


Concept: T. Clayton, D. Bruederle  
Hardware Implementation: T. Clayton, D. Bruederle



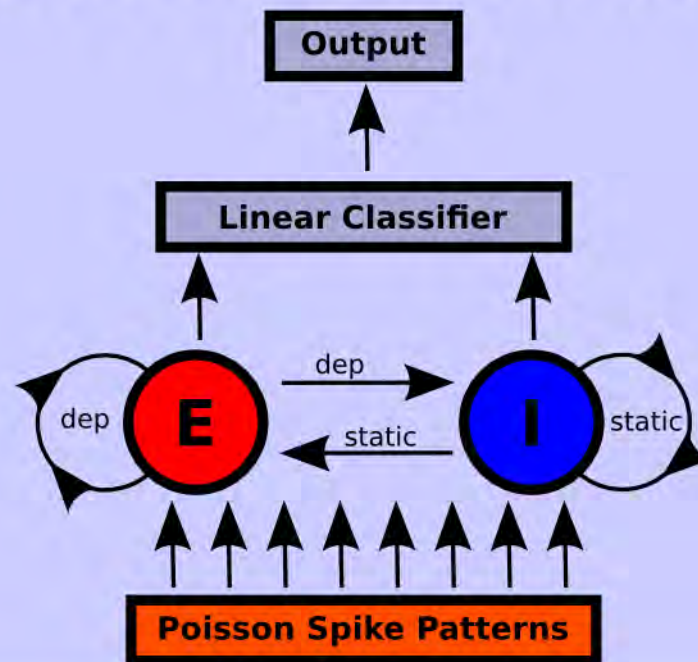
Concept: T. Clayton, D. Bruederle  
 Hardware Implementation: T. Clayton, D. Bruederle

# Layer 2/3 Attractor Model



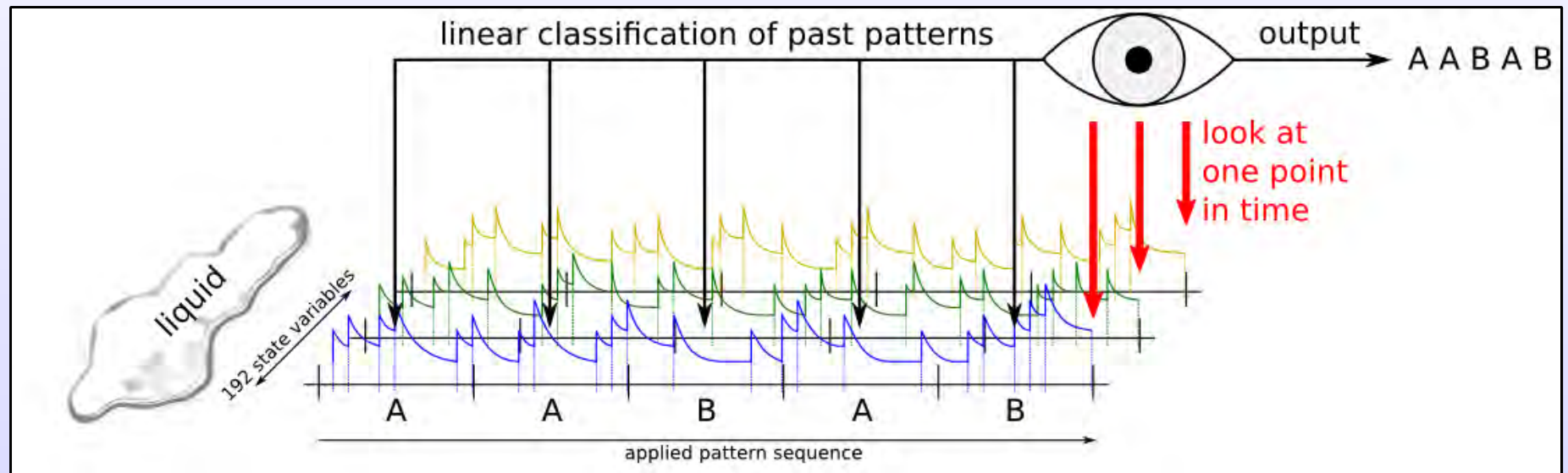
*Attractor Dynamics in a Modular Network Model.* Mikael Lundqvist, Martin Rehn, Mikael Djurfeldt, Anders Lansner. *Network: Computation in Neural Systems*, 17, 253-276, 2006.  
Hardware Implementation: M. Petrovici, D. Bruederle

# Liquid State Machine



*On the computational power of circuits of spiking neurons.* W. Maass, T. Natschlaeger, H. Markram. Journal of Physiology (Paris), 2004.

Hardware Implementation: J. Bill, S. Jeltsch, B. Vogginger, M. Albert, M. Petrovici



*On the computational power of circuits of spiking neurons.* W. Maass, T. Natschlaeger, H. Markram. *Journal of Physiology (Paris)*, 2004.  
 Hardware Implementation: J. Bill, S. Jeltsch, B. Vogginger, M. Albert, M. Petrovici



# **Special Thanks to**

## **Script Contributions and Experiments**

Marvin Albert, Johannes Bill, Thomas Clayton, Sebastian Jeltsch, Jens Kremkow, Pradeep Krishnamurthy, Anders Lansner, Mikael Lundqvist, Mihai Petrovici, Bernhard Vogginger

## **Coordination of the `NeuralEnsemble.org` Initiative**

Andrew Davison, Eilif Muller