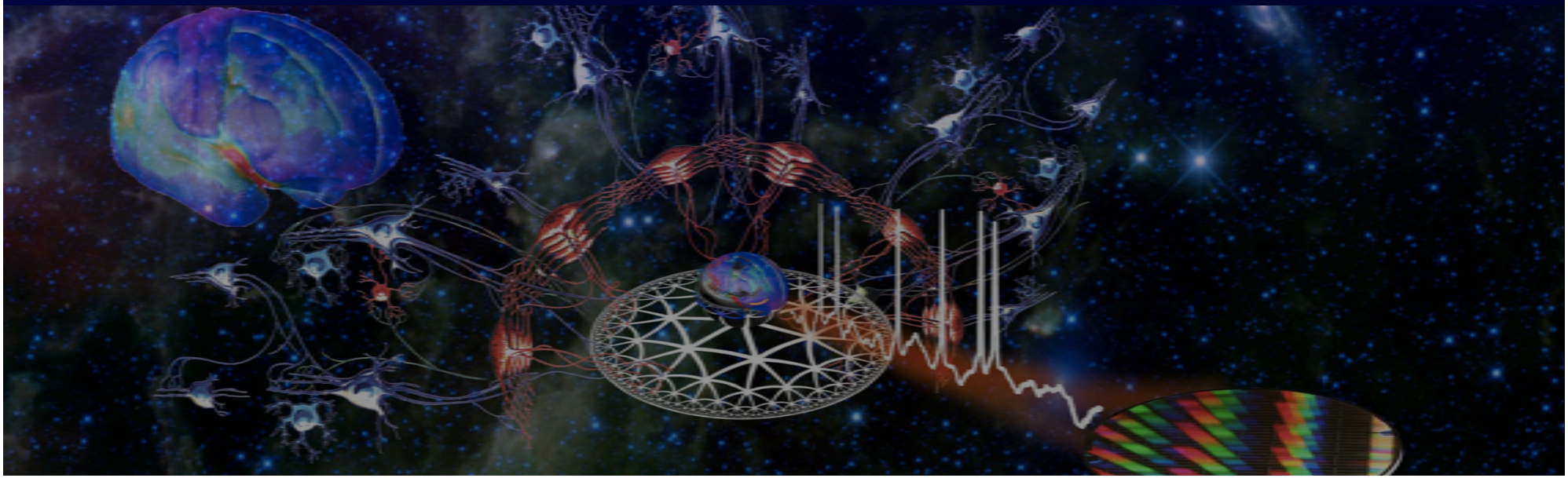
FRONTIERS IN NEUROMORPHIC COMPUTATION:
a Multi-FACETS Enterprise
3 - 4 JUNE 2010

Where do we go from here ?

Karlheinz Meier



FACETS – Personal conclusions

Science

-

Technology

Functional, user friendly multichip systems
New circuit concepts and demonstrators (neurons, synapses, storage)
High speed asynchronous communication concepts and demonstrators
Wafer scale integration and connection technologies

Integration

PyNN – A platform indepedent neural network language
Databases
Experimental protocolls and platforms

Community Building

Working, proven and sustainable interdisciplinary collaboration
Successful collaboration for follw-up projects

Graduate Education

More than 100 PhD students
New Marie-Curie graduate school

What's next ?

Brain-i-Nets

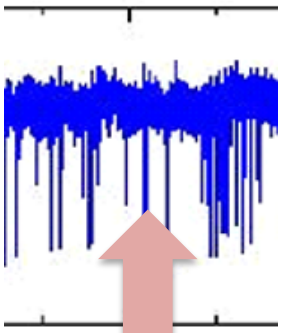
Started this year :
Learning and plasticity

Started last year :
Graduate Students

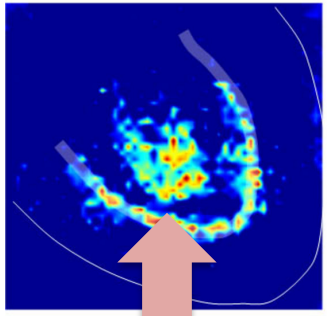
On the move :

FACETS follow-up

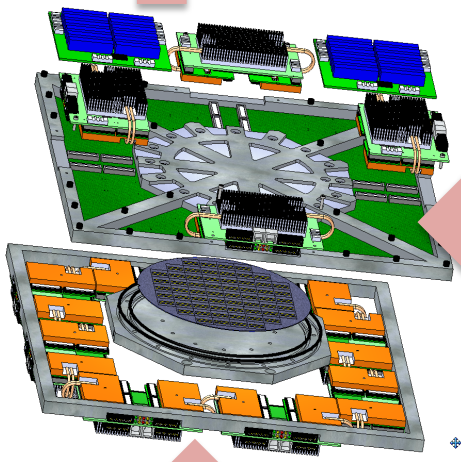
FET-Flagship



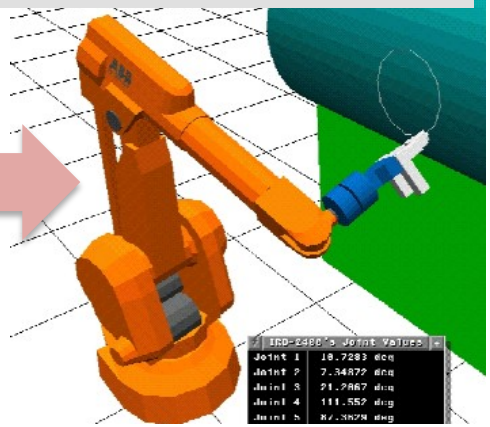
Output of biologically equivalent data



Hybrid (Neuromorphic-HPC) Multiscale Modelling



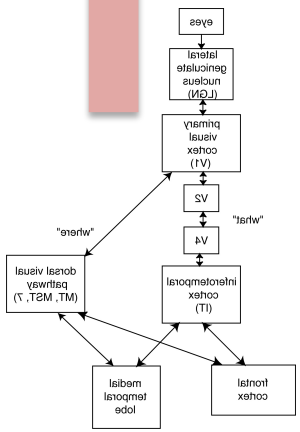
Virtual environment



$$c_{\mathrm{m}} \frac{dV}{dt} = -g_{\mathrm{leak}}\left(V - E_{\mathrm{l}}\right)$$

$$\Delta t = t_{\mathrm{post}} - t_{\mathrm{pre}}$$

Input of microscopic and macroscopic theory



Microscopic – macroscopic

Milliseconds – years

Rapid cycling of experiments

SUPERFACETS ?

Base Facility
24 crates with
312 wafer assemblies

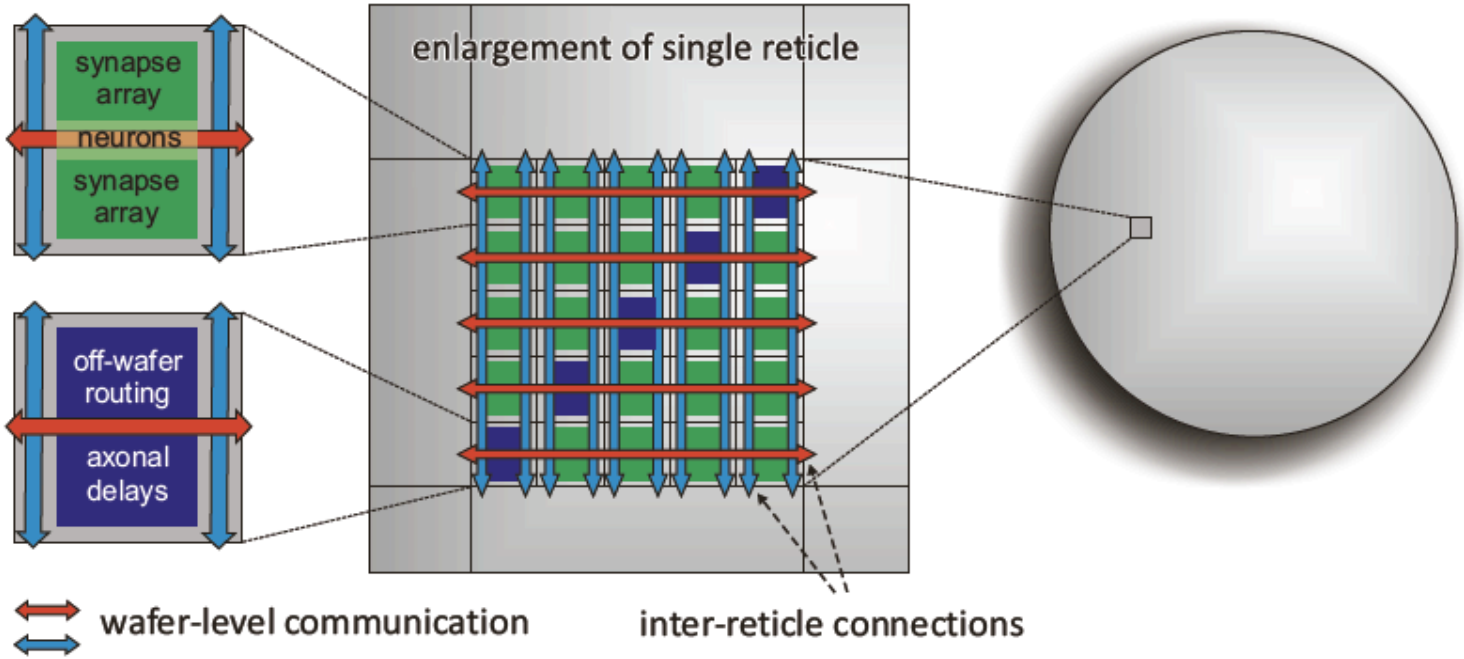
With current 60 nm technology

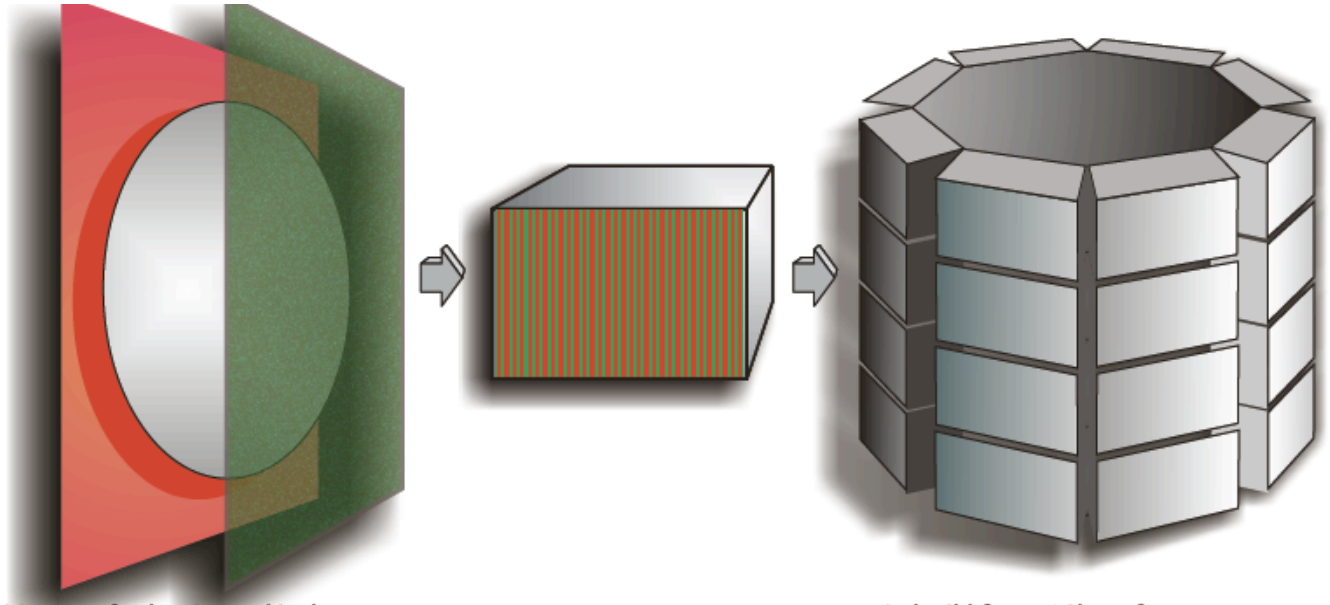
10^9 Multic. Neurons
10^{13} dynamic synapses

Full Readout and Configurability

Technology Upgrades

- Increase Number of Base Facilities
- Increase Component Density

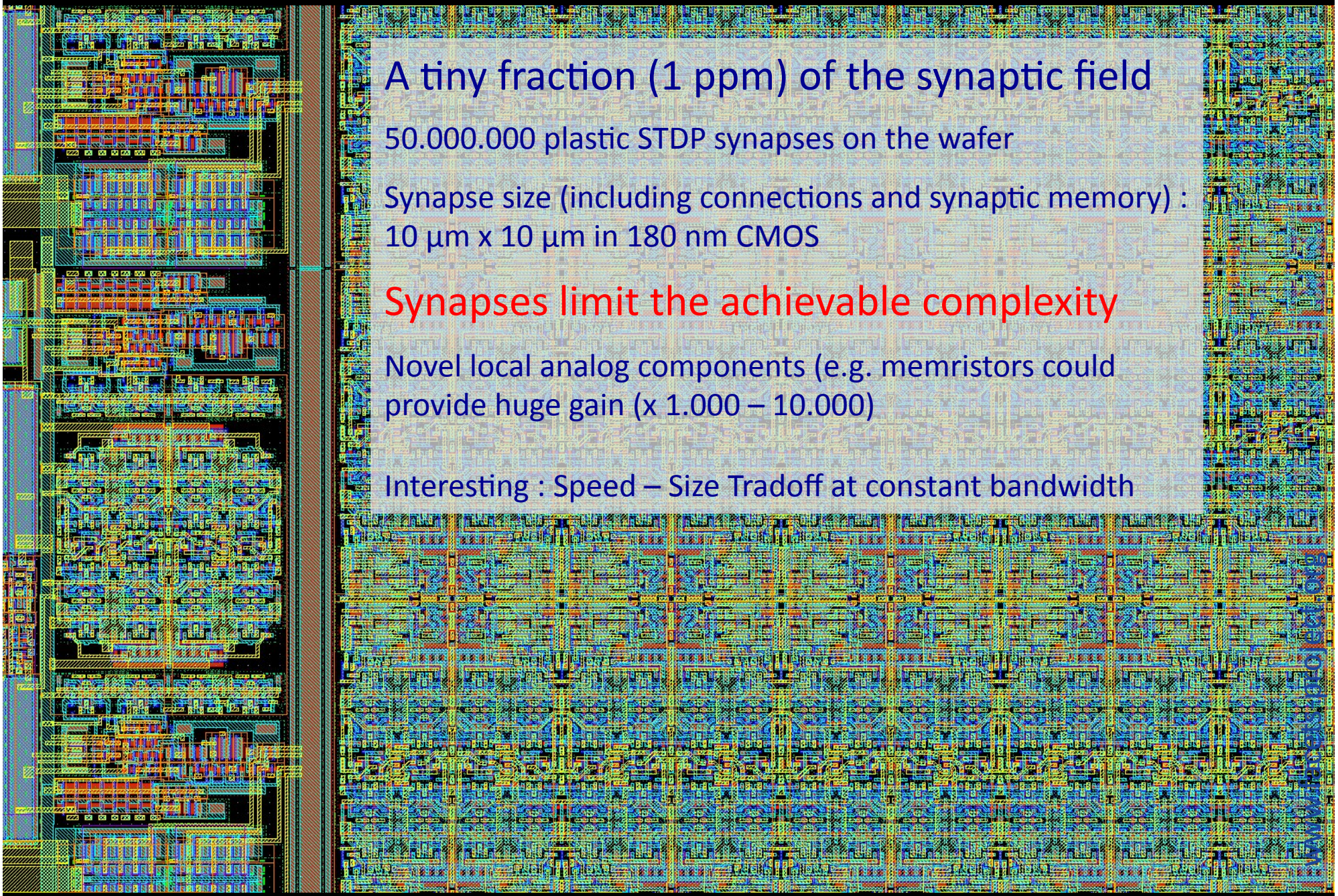


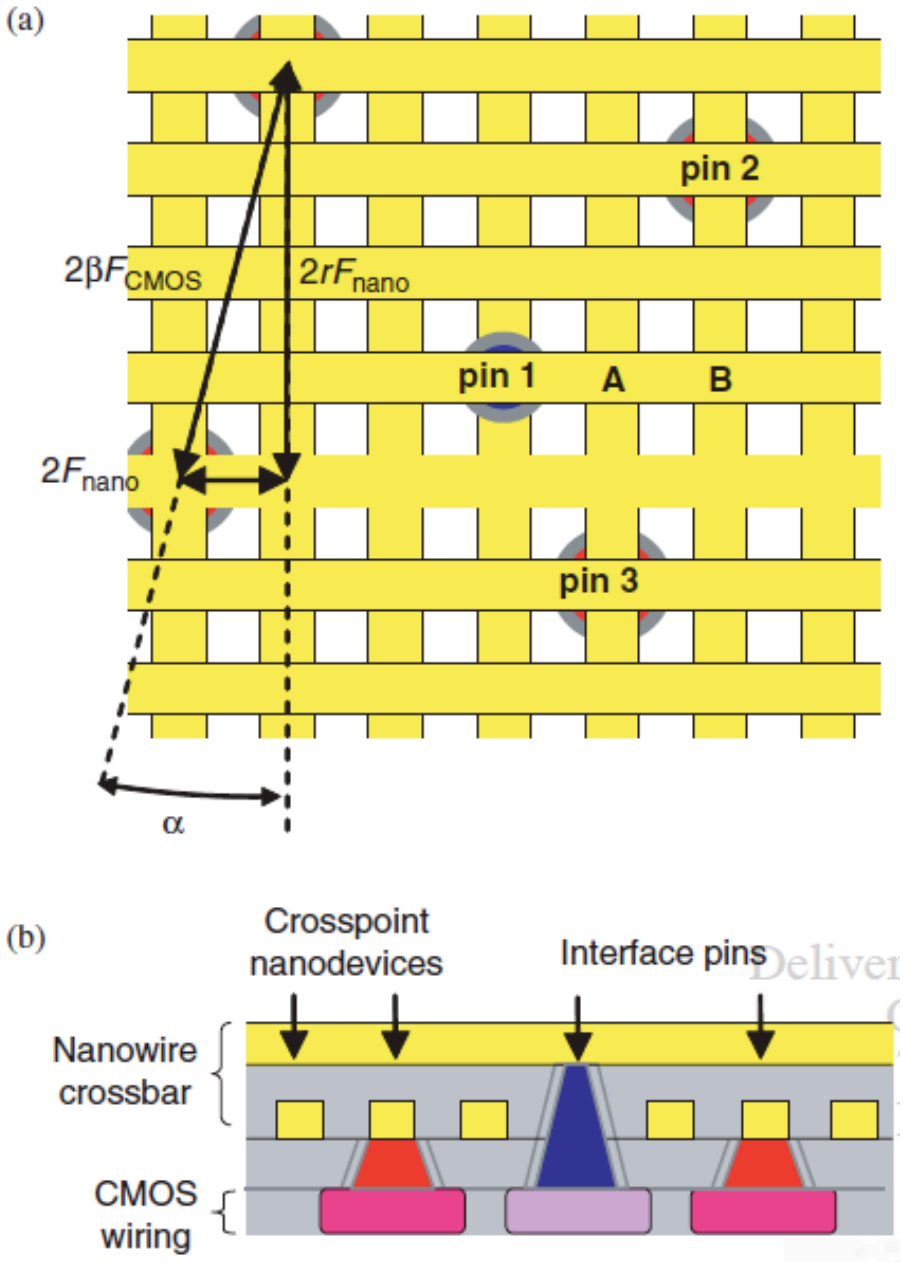


30cm wafer laminated in-between copper cooling base and multi-layer PCB. Total assembly thickness: <2mm

312 wafer assemblies mounted in one crate

NCF build from 10k wafers: four layers of eight crates arranged in a cylindrical fashion to minimize inter-connection distances


A tiny fraction (1 ppm) of the synaptic field
50.000.000 plastic STDP synapses on the wafer
Synapse size (including connections and synaptic memory) :
10 µm x 10 µm in 180 nm CMOS
Synapses limit the achievable complexity
Novel local analog components (e.g. memristors could provide huge gain (x 1.000 – 10.000)
Interesting : Speed – Size Tradoff at constant bandwidth



K. Likharev, Journal of Nanoelectronics and Optoelectronics, Vol.3, 203–230, 2008

Basic Idea : CMOL

Take the best of best worlds : CMOS **fidelity** + Nanoscale **density**

2 Terminal Cross-Point Devices

Nanowire Cross Bars on Top of conventional CMOS devices

Approx. 1000-10000 fold synaptic density

1000-10000 fold communication bandwidth requirement !

Speed vs. Density

THANKS TO ALL OF YOU FOR A WONDERFUL AND EXCITING PROJECT !!!

We came a long way in the last 5 years !

1st FACETS plenary meeting, INRIA, 2005